AMENDMENTS TO THE CLAIMS

1. (currently amended) A memory unit for use in an integrated circuit (IC) comprising:

an array of memory cells;

a first data transfer interface coupled to the array of memory cells to provide a first access path for a processor and a subsystem of the IC to access said array of memory cells;

a second data transfer interface coupled to the array of memory cells to provide a second access path for said processor to access said array of memory cells, the second access path to provide access to at least one memory cell accessible through the first access path; and

a controller coupled to the array of memory cells and the first and second data transfer interfaces to control said array of memory cells and said first and second data transfer interfaces to facilitate accesses of said memory unit by said processor and said subsystem.

2. (original) The memory unit of claim 1, wherein said first data transfer interface comprises

a first inbound queue coupled to said array of memory cells for queuing a first plurality of memory accesses of said processor and said subsystem of a first priority;

a second inbound queue coupled to said array of memory cells for queuing a second plurality of memory accesses of said processor and said subsystem of a second priority; and

an outbound queue coupled to said array of memory cells for queuing output responses to said first and second plurality of memory accesses of said processor and said subsystem of said first and second priorities accessed through said first and second inbound queues.

3. (original) The memory unit of claim 1, wherein said second data transfer interface comprises

an inbound queue coupled to said array of memory cells for queuing a first plurality of memory accesses of said processor; and

an outbound queue coupled to said array of memory cells for queuing output responses to said first plurality of memory accesses of said processor.

4. (previously presented) The memory unit of claim 1, wherein said controller comprises

a sequential storage structure coupled to said array of memory cells;

a multiplexor coupled to inbound queues of said first and second data transfer units and said sequential storage structure to sequence memory accesses queued in said inbound queues into said sequential storage structure; and

a state machine coupled to said sequential storage structure and said multiplexor to control their operation.

5. (original) The memory unit of claim 4, wherein said state machine controls said multiplexor to sequence memory accesses queued in said second data transfer interface into said sequential storage structure before sequencing any memory access queued in said first data transfer interface into said sequential storage structure.

6. (original) The memory unit of claim 4, wherein said state machine controls said multiplexor to sequence memory accesses queued in inbound queues of said first data transfer interface into said sequential storage structure, in accordance with assigned priorities of said inbound queues.

7. (original) The memory unit of claim 1, wherein said controller comprises

a first sequential storage structure to stage headers for output responses to memory accesses;

a second sequential storage structure coupled to said array of memory cells to stage output responses to memory accesses;

a first multiplexor coupled to said first and second sequential storage structures to selective output one of said staged headers of output responses to memory accesses and said staged output responses to memory accesses;

a second multiplexor coupled to said first multiplexor and outbound queues of said first and second data transfer units to selective output the selected output of said first multiplexor to a selected one of said outbound queues of said first and second data transfer unit; and a state machine coupled to said first and second sequential storage structures, said first and second multiplexors, and said outbound queues of said first and second data transfer units to control their operation.

8. (original) In a memory unit of an integrated circuit (IC), a method of operation comprising:

queuing first memory accesses of a processor and a plurality of subsystems of the IC in inbound queues of a first data transfer interface;

queuing second memory accesses of the processor in an inbound queue of a second data transfer interface; sequencing said first and second memory accesses into a single sequence of memory accesses; and

servicing said first and second memory accesses in accordance with their sequence order.

9. (original) The method of claim 8, wherein said queuing of said first memory accesses of a processor and a plurality of subsystems of the IC in inbound queues of a first data transfer interface comprises

queuing said first memory accesses into inbound queues of said first data transfer interface having associated priorities, in accordance with priorities of said first memory accesses.

10. (original) The method of claim 8, wherein said sequencing comprises

sequencing second memory accesses queued in said second data transfer interface before sequencing any memory access queued in said first data transfer interface.

11. (original) The method of claim 8, wherein said sequencing comprises sequencing first memory accesses queued in inbound queues of said first data transfer interface, in accordance with assigned priorities of the inbound queues.

12. (original) The method of claim 8, wherein said servicing comprises generating and queuing headers for output responses to said first and second memory accesses.

13. (original) The method of claim 8, wherein said servicing comprises queuing output responses to said first and second memory accesses.

14. (original) The method of claim 8, wherein said servicing comprises merging headers for output responses to said first and second memory accesses and output responses to said first and second memory accesses.

15. (original) The method of claim 8, wherein said servicing comprises selectively outputting headers for output responses to said first and second memory accesses and output responses to said first and second memory accesses to a selected one of said first and said second data transfer interfaces.

16. (currently amended) An integrated circuit comprising:
a processor;
a plurality of subsystems; and
a memory unit coupled to said processor and said subsystems having at least a first access path to facilitate access by said processor and said subsystems to access said memory unit and a second access path to facilitate access by said processor to at least one memory cell that is also accessible through the first access path.

17. (previously presented) The integrated circuit of claim 16, wherein said memory unit comprises
an array of memory cells;
a first data transfer interface coupled to the array of memory cells to provide said first access path for said processor and said subsystems;
a second data transfer interface coupled to the array of memory cells to provide said second access path for said processor; and
a controller coupled to the array of memory cells and the first and second data transfer interfaces to control said array of memory cells and said first and second data transfer interfaces.

18. (original) The integrated circuit of claim 17, wherein said first data transfer interface comprises

a first inbound queue coupled to said array of memory cells for queuing a first plurality of memory accesses of said processor and said subsystem of a first priority;

a second inbound queue coupled to said array of memory cells for queuing a second plurality of memory accesses of said processor and said subsystem of a second priority; and

an outbound queue coupled to said array of memory cells for queuing output responses to said first and second plurality of memory accesses of said processor and said subsystem of said first and second priorities accessed through said first and second inbound queues.

19. (original) The integrated circuit of claim 17, wherein said second data transfer interface comprises

an inbound queue coupled to said array of memory cells for queuing a first plurality of memory accesses of said processor; and

an outbound queue coupled to said array of memory cells for queuing output responses to said first plurality of memory accesses of said processor.

20. (original) The integrated circuit of claim 17, wherein said controller comprises

a sequential storage structure coupled to said array of memory cells;

a multiplexor coupled to inbound queues of said first and second data transfer units and said sequential storage structure to sequence memory accesses queued in said inbound queues into said sequential storage structure; and

a state machine coupled to said sequential storage structure, said multiplexor, and said inbound queues of said first and second data transfer units to control their operation.

21. (original) The integrated of claim 20, wherein said state machine controls said multiplexor to sequence memory accesses queued in said second data transfer interface into said sequential storage structure before sequencing any memory access queued in said first data transfer interface into said sequential storage structure.

22. (original) The integrated circuit of claim 20, wherein said state machine controls said multiplexor to sequence memory accesses queued in inbound queues of said first data transfer interface into said sequential storage structure, in accordance with assigned priorities of said inbound queues.

23. (original) The integrated circuit of claim 17, wherein said controller comprises

a first sequential storage structure to stage headers for output responses to memory accesses;

a second sequential storage structure coupled to said array of memory cells to stage output responses to memory accesses;

a first multiplexor coupled to said first and second sequential storage structures to selective output one of said staged headers of output responses to memory accesses and said staged output responses to memory accesses;

a second multiplexor coupled to said first multiplexor and outbound queues of said first and second data transfer units to selective output the selected output of said first multiplexor to a selected one of said outbound queues of said first and second data transfer unit; and

a state machine coupled to said first and second sequential storage structures, said first and second multiplexors, and said outbound queues of said first and second data transfer units to control their operation.

24. (original) The integrated circuit of claim 16, wherein said integrated circuit further comprises an on-chip bus to which said memory unit and at least a subset of said subsystems are attached.

25. (original) The integrated circuit of claim 16, wherein said integrated circuit further comprises

a data traffic router to which said memory unit, said processor, and at least one of said subsystems is attached, said data traffic router facilitating concurrent communication between selected combinations of said memory unit, said processor and said at least one subsystem.

26. (previously presented) The integrated circuit of claim 16, wherein each of said subsystems is a security engine, a voice processor, a collection of peripheral device controllers, a framer processor, a network media access controller, or an external device controller.

27. (currently amended) In an integrated circuit (IC), a method of operation comprising:

a processor and a plurality of subsystems of the IC successively making first memory accesses of a memory unit of the IC via a first access path in turn;

the processor also successively making second memory accesses to said memory unit via a second access path, dedicated to the processor, in parallel; and

the memory unit servicing said first and second memory accesses made through said first and second access paths ~~in parallel~~.

28. (original) The method of claim 27, wherein said servicing comprises

queuing said first memory accesses of said processor and said plurality of subsystems of the IC in inbound queues of a first data transfer interface of said memory unit;

queuing said second memory accesses of the processor in an inbound queue of a second data transfer interface of said memory unit;

sequencing said first and second memory accesses into a single sequence of memory accesses; and

servicing said first and second memory accesses in accordance with their sequence order.

29. (original) The method of claim 28, wherein said queuing of said first memory accesses of said processor and said plurality of subsystems of the IC in inbound queues of a first data transfer interface comprises

queuing said first memory accesses into inbound queues of said first data transfer interface having associated priorities, in accordance with priorities of said first memory accesses.

30. (original) The method of claim 28, wherein said sequencing comprises

sequencing second memory accesses queued in said second data transfer interface before sequencing any memory access queued in said first data transfer interface.

31. (original) The method of claim 28, wherein said sequencing comprises

sequencing first memory accesses queued in inbound queues of said first data transfer interface, in accordance with assigned priorities of the inbound queues.

32. (original) The method of claim 28, wherein said servicing comprises

generating and queuing headers for output responses to said first and second memory accesses.

33. (original) The method of claim 28, wherein said servicing comprises

queuing output responses to said first and second memory accesses.

34. (original) The method of claim 28, wherein said servicing comprises

merging headers for output responses to said first and second memory accesses and output responses to said first and second memory accesses.

35. (original) The method of claim 28, wherein said servicing comprises

selectively outputting headers for output responses to said first and second memory accesses and output responses to said first and second memory accesses to a selected one of said first and said second data transfer interfaces.

36. (original) The method of claim 27, wherein the method further comprises

a first of said subsystem notifying said processor with respect to said first subsystem having placed a first data in said memory unit;

said processor making a first access of said first subsystem, and awaiting for a first reply to said first access of said first subsystem; and

said processor making a second access of said memory unit via said second access path for said first data placed into said memory unit by said first subsystem after at least receiving said first reply for said first access of said first subsystem.

37. (original) The method of claim 38, wherein the method further comprises

said processor making a second access of said memory unit via said first access path, and awaiting for a second reply to said second access of said memory unit; and

said processor making said first access of said memory unit via said second access path for said first data placed into said memory unit by said first subsystem after also receiving said second reply for said second access of said memory unit.

38. (original) The method of claim 27, wherein the method further comprises

a first of said subsystem notifying said processor with respect to said first subsystem having placed a first data in said memory unit;

said processor making a first access of said memory unit via said first access path, and awaiting for a first reply to said first access of said memory unit; and

said processor making a second access of said memory unit via said second access path for said first data placed into said memory unit by said first subsystem after at least receiving said first reply for said first access of said memory unit.

39. (new) The memory unit of claim 1, further comprising:

a multiplexor coupled to the first and second data transfer interfaces to sequence memory accesses from the first and second data transfer interfaces.

40. (new) The memory unit of claim 1, wherein the second data transfer interface is an interface dedicated to memory accesses from the processor.